Switched Capacitor Bandpass Filter Tuned by Ring VCO in CMOS 0.35 µm

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Abstract — **Recently Switched-Capacitor filtering capabilities have grown to the Megahertz frequency range. This paper describes an original association of a switched capacitor (SC) bandpass filter and its command circuit made up by a ring voltage controlled oscillator (VCO) with "exclusive-or" (XOR) gates. Implemented in a standard BiCMOS 0.35 µm technology, this circuit is attended to be employed in a subset of mobile phone applications using the Tetrapol standard of EADS-TELECOM, which requires a frequency range between 380 and 520 MHz. The results presented for this first design are a tunable center frequency range equal to 220 MHz (320 MHz – 540 MHz), with a quality factor greater than 300.**

I. Introduction

The association proposed in this paper presents significant advantages and consequently should render this kind of SC filter much more attractive for the radio communications system especially for zero IF receivers.

This circuit would bring two main advantages to high frequency systems: the possibility of tuning on a broad frequency band allowing to sweep different channels and the high quality factor which reach few hundreds. The critical limitation of the SC filters is related to the construction of the command circuit of the switches, which was generally carried out using a shift register. This solution which required a clock frequency equal to the center frequency of the filter multiplied by the number of cells to commutate is exclusively used at low frequencies.

The behavioral analysis of these circuits requires the development of an algorithm based on the conversion matrices formalism, which consists in the linearisation of the non-linear elements around the large signal operation point [1]. This method of analysis has been used to be the most rigorous and the most effective in term of calculating time (CPU), both for the filter transfer function and the phase noise oscillator analysis [2,3]. The results presented in the present paper, are provided by the ADS software (Agilent), which uses this formalism.

II. General Principle Of SC Filters And Their Command Circuit

The N cells of the SC filter (Fig.1) are successively activated by the command signals applied to the switches.

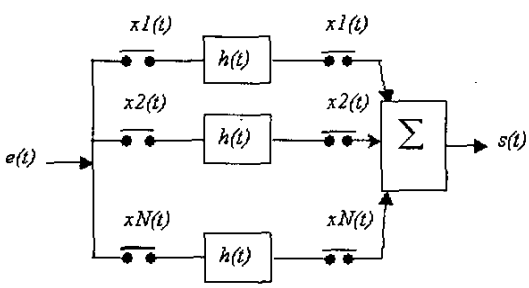

Fig. 1. General structure of the filter.

These cells are identical R-C lowpass filters. Their transfer function and impulse response are respectively noted $H(f)$ and $h(t)$. In a first approach, the command signals of the switches are considered to be Dirac's impulses $\delta(t)$ spaced by a period To. Then, the total transfer function $Hs(f)$ of the filter is the result of the transfer function of the elementary lowpass filter transposed around the frequency $Fo=1/To$ and all its harmonics components. Actually, this behavior undergoes a correction in $sinx/x$, due to the cyclic ratio of the command signals, which are not ideal Dirac impulses, and which have To/N duration. An example is given in Fig.2, with R and C values are respectively *1 kOhm* and *50 pF*, for a switching frequency of *500 MHz* with ideal switches. This Fig.2 shows high selectivity and dynamic performances.

For reasons related to the complexity of the realization at very high frequencies and particularly to the difficulty for switching, the proposed circuit has the configuration shown in Fig.3.

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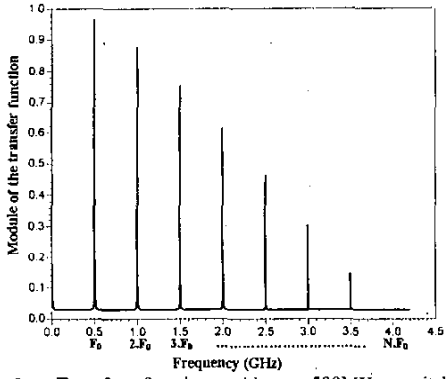

Fig. 2. Transfer function with a 500MHz switching frequency.

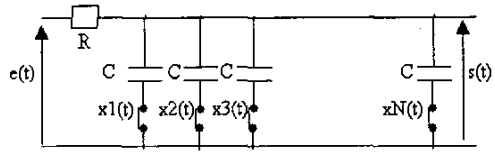

Fig. 3. Switched capacitor filter.

The switches are successively closed with a switching period *To*, during a time *To/N*. These filters can be used for clock recovering by filtering the harmonic components. They can also be employed as bandpass filter centered at *Fo*. This last application will be taken into account in the present paper.

From Fig.3, the quality factor can be expressed by the following simplified form $Q=\pi.N.R.C.Fo$ This expression shows that the quality factor depends directly of the number of cells *N*. The number of eight cells that is retained for this study seems to be a good trade off between the quality factor and chip complexity, which quickly increases with *N*.

The SC filter described in this paper has three substantial advantages:

High quality factor: the bandwidth is directly related with the lowpass circuit bandwidth divided by the number of cells

Agility: the adjustment of the center frequency depends on the switching frequency and can thus be tuned by an internal or external system.

Integration: The circuit is fully integrated on one chip.

All these advantages are closely related to the possibility to generate switching signals at high frequencies.

The original solution proposed in this paper uses a ring oscillator associated with "or-exclusive" (XOR) gates.

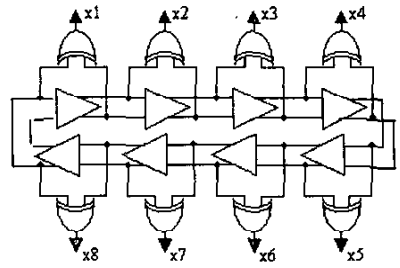

Fig. 4. Command circuit.

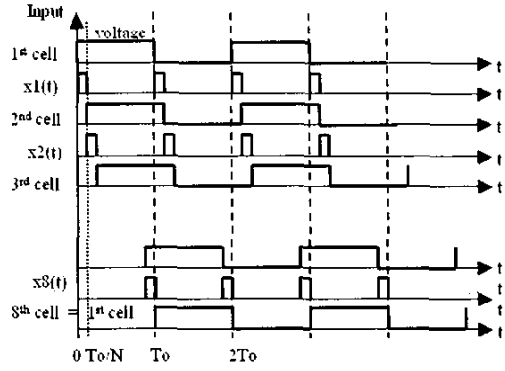

Fig. 5. Theoretical waveforms of the command circuit.

The *N* cells ring VCO generates signals with a period of *2.To*. For each cell, the input and output signals are delayed of *To/N* (Fig. 5). Then, the input and output of each ring VCO delay cell are applied to an "or-exclusive" (XOR) gate for getting a *To/N* duration impulse, which is repeated at all the half-periods.

This original solution allows to design a command circuit at *Fo/2*, whereas the others using a shift register require a clock frequency at *NFo*. Thus the oscillation frequency *Fosc* required for the command circuit is decreased by a *1/(2.N)* ratio.

III. Full Circuit Design

All the following results are obtained by using the ADS software and the models are provided by ALCATEL Microelectonics foundry.

A. Ring VCO

The ring VCO comprises eight identical differential delay cells. Each cell is based on NMOS transistors differential pair which generates the necessary gain and the delay for allowing the oscillation phenomena. The

delay cumulated with the eight cells gives a total of *2.To*, so that the oscillation frequency is *1/(2Fo)*. The delay generated by one cell depends of a time-constant *R.Cp*. The *R* resistance corresponds to the differential resistive load which is gotten by PMOS transistors working in triode operation region. The *Cp* capacitance is due to the capacitor placed between drain and source of each PMOS transistor. The frequency tuning is obtained by controlling both the common current source and the bias point of the PMOS transistors which modify the *R* value.

The gate size of NMOS transistors is $4x6x0.35\ \mu m^2$ and PMOS transistors gate size is $3x4x0.35\ \mu m^2$. The output frequency of this ring VCO is adjustable between 160 MHz and 270 MHz by controlling the current source of the delay cells. For this ring VCO, a special attention was given to its temporal waveform signals [4] in order to limit the jitter and hence the phase noise roughly to –111 dBc/Hz at 1 MHz of the offset frequency. It will be interesting to associate this VCO with a Phase Locked Loop to reduce the phase noise.

B. "OR exclusive" gates

The goal of the XOR gates is to generate impulse commands from the delay cells outputs which provide useful 0° and 180° signals.

Moreover, in order to respect symmetry of the ring VCO delay cells, the input XOR gates are identical and consequently present the same input impedance. The XOR gates input impedance values must be higher than the delay cells loads for not modifying the elementary time-constant. This objective is achieved by using $1x1x0.35\ \mu m^2$ size gate NMOS. Nevertheless, these transistors with low dimension gates, cannot provide the necessary current to drive the switching transistors, which have a gate width of $6x25\ \mu m$ for a length of $0.35\ \mu m$. Consequently, a buffer consisted of five stages allows to ensure the switching.

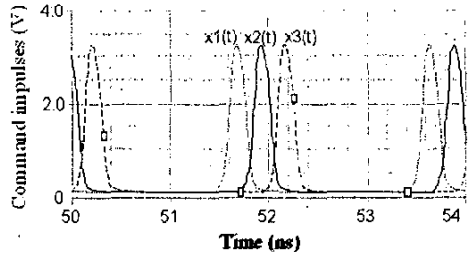

Fig. 6. Command signals x1(t), x2(t) and x3(t) for a switching frequency closed to 500 MHz.

Fig. 6 presents the command signal waveforms x1(t), x2(t) ant x3(t) applied to the first second and third switches. The impulse magnitude is higher than 3 Volts, allowing to get a low Ron value of the switch.

During the design, it is necessary to avoid the insertion losses generated by the impulses recovering.

C. Switched Capacitor Filter

The switches are realized with NMOS transistors sequentially controlled in ON-OFF state (Fig.7).

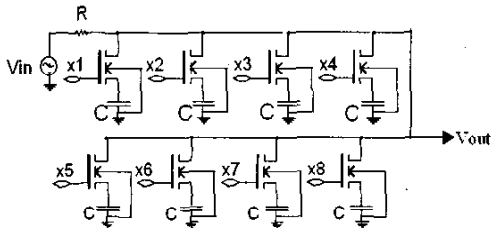

Fig. 7. Filter schematic.

The elementary transfer function presents a pole to the numerator. This pole compensates the slope of the elementary lowpass filter transfer function and thus the attenuation remains constant. The choice of the switches size being critical and it should be optimized. Indeed, with a large width gate of switched transistor insures a low *Ron* resistance, and a considerable parasitic capacitance *Cds*, under this condition, the system bandwidth is limited by the cut-off frequency $Fc=1/(2\pi R.N.Cds)$ and the dynamic of the filter is attenuated. With a small width gate, the *Cds* value is low but the *Ron* resistance value is important. Under this condition, the dynamic of the filter is still degraded by the increasing of the "floor". The used transistors are channel N MOSFETs of six fingers having each one a gate width of $25\ \mu m$ and a length of $0.35\ \mu m$. These transistors present a resistance *Ron* of *30* Ω and a drain-source capacitance *Cds* of 0.06pF. It results an optimal dynamic of the gain voltage equal to 27 dB which is between a voltage gain of –3 dB in the bandwidth and –30 dB in the rejection band.

To improve the dynamic transfer function, an inductor replaces the input resistor. This innovation produces two benefits: (1) the improvement of the dynamic behavior, by compensating the *Cds* capacitances, (2) the reduction of the noise figure. The insertion losses and consequently the dynamic range are better and reached very good performances.

The *LC* filter configuration presents an adjustable center frequency ranging between 320 MHz and 540

MHz with a bandwidth of 900 kHz and a quality factor ranging between 330 and 625 according the center frequency. The table I indicates the main simulation results of both the *LC* and *RC* configurations.

TABLE I
SIMULATION RESULTS

Parameters	*LC conf.*	*RC conf.*
Tuning frequency range (MHz)	250-500	250-500
Frequency Bandwidth (KHz) @3dB	900	900
Insertion loss @ Fo (dB)	2.5	10
Rejection losses@Fo/2 (dB)	28	31
1dB Input compression point @ Fo (dBm)	-5	-12.5
Noise Figure @ Fo (dB)	7	19

IV. MEASUREMENTS

The measured oscillation frequency Fosc is in the 120-254 MHz range. Consequently the center frequency band is 240-508 MHz. An external network allows an input and output *50 Ω* matching. Fig. 8 shows the measured switched capacitor filter transfer function, at 300 MHz center frequency. The selectivity can be improved by decreasing the switching signals magnitude. In these conditions, the bandwidth becomes equal to 0.97 MHz (0.9 MHz simulation result). The quality factor obtained is then roughly 310.

The first measurement results at a center frequency of 300 MHz are synthesized in the table II.

The obtained results with this first trial are very interesting. The required performances are reached, only the dynamic must be improved. This filter is fully integrated and the center frequency can be controlled with an internal clock signal.

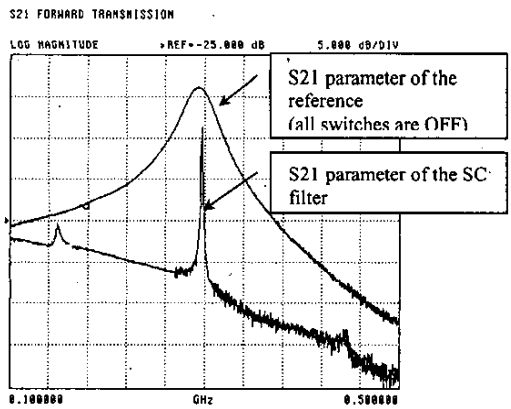

Fig. 8. Measured Transfer function.

TABLE II
MEASUREMENT RESULTS

Parameters	Meas. 1
Power Supply (Volt)	3
Spurious rejection min (dB)	18
Frequency bandwidth @ -3 dB (MHz)	0.970
Quality factor	310
Insertion loss @ Fo (dB)	4
1 dB input compression point @ Fo(dBm)	-9

V. CONCLUSION

An original association of a ring VCO controlling a switched capacitor filter is proposed. The results obtained with this circuit are very interesting, in particular the frequency range and the selectivity.

To ensure the development of switched capacitor circuits, a technological compromise must be made, between an expensive powerful technology in order to obtain more attracting results, and a less powerful technology with the risk to degrade the filter performances and render them not-competing when compared with the passive circuits. This study shows the feasibility of these filters in MOSFET technology for RF applications, in particular for the mobile phone domain.

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